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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,033	07/03/2003	Tadashi Iguchi	03180.0326	5852

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,033	IGUCHI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,5,7-11 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,15 and 22* is/are allowed.

6)☒ Claim(s) *4,7-11,14 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 4, 7-11, 14, and 16-21 is withdrawn in view of Aritome (USPN 5,949,101) and Hagiwara (JP 2001-274367). Rejections based on these references follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 7-11, 14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aritome (USPN 5,949,101).

4. In reference to claim 4, Aritome (USPN 5,949,101) discloses a similar device. Figures 6A and 12G of Aritome each discloses a non-volatile semiconductor memory device with memory cells arranged in a matrix on a semiconductor substrate (1A, 40). Each cell in the matrix has a floating gate or electrode (4, 30). A plurality of first trenches are formed in the semiconductor substrate (1A, 40) with each first trench being formed between the memory cells adjacent each other along a gate width direction. The plurality of first trenches is filled with an isolating filler (2, 12). There is a plurality of second trenches formed in the isolating filler between the floating gates (4, 30) of the

memory cells adjacent to each other along the gate width direction. A word line (6, 75), buried in the second trenches, is connected to the memory cells and extends along the gate width direction. Aritome does not each the exact trench shape as claimed by the applicant. However:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Therefore this claim is not patentable over Aritome.

5. In reference to claim 7, figure 6 of Aritome shows a gate insulating film (33) in the second trenches. The wordline (6) is on the gate insulating film (33).

6. With regard to claim 8, Aritome discloses that the gate insulating film (33) may be made of silicon nitride (claims 11 and 16 in column 16).

7. In reference to claim 9, the first and second trenches of Aritome have approximately the same top diameter. However the second trench of Aritome has bottom diameter which is smaller than that of the first trench. Thus Aritome has ratio of a top diameter to a bottom diameter of the second trench which is greater than the ratio of a top diameter to a bottom diameter of the first trench.

8. In reference to claim 10, the second trench is shallower than the first trench and extends below a surface of the semiconductor substrate (1A).

9. With regard to claim 11, the non-volatile memory device in figure 6A is a NAND type electrically erasable programmable read only memory (column 7, lines 20-25).

10. In reference to claim 18, figure 6 of Aritome shows that there is a second gate insulating film (33) on the inner surface of each of the second trenches.

11. With regard to claim 21, the applicant has characterized a second trench which is capable of reducing parasitic capacitance as being shallower than the first trench and preferably reaches at least the surface of the well region (currently filed specification, p. 9, lines 16-21). The second trench of Aritome meets these characteristics thus meeting the claim. Furthermore, the applicant has characterized a second trench as reducing parasitic capacitance since the parasitic capacitance generated by the floating gate, the dielectric in the trench, and an insulating film of the trench, and at the word line is electrically connected in parallel to the parasitic capacitance between floating gates of the memory cells (currently filed specification, p. 3, lines 6-16). The second trench of Aritome also meets these characteristics as well and thereby meets the claim.

12. In reference to claim 14, Aritome (USPN 5,949,101) discloses a similar process. Figures 6A and 12G of Aritome each discloses a method of manufacturing a semiconductor memory which comprises making element isolating regions (2, 12) by forming a plurality of first trenches in a semiconductor substrate (1A, 40). Each first trench is made between adjacent ones of memory cell forming regions along a gate width direction. The plurality of first trenches is filled with a plurality of isolating fillers. A plurality of floating gate electrodes (4, 30) are formed on the semiconductor substrate (1A, 40) at the memory cell forming regions. The floating gate electrodes (4, 30) have a predetermined gate width. A plurality of second trenches is formed in the isolating fillers filled in the first trenches. Each second trench is made between adjacent ones of the floating electrodes (4, 30) along the gate width direction. A word line (6, 75) is formed in the second trenches. The wordline (6, 75) is connected to the memory cells and

extends along the gate width direction. Aritome does not each the exact trench shape as claimed by the applicant. However:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Therefore this claim is not patentable over Aritome.

13. With regard to claim 16, the second trenches are in self-alignment with the floating electrodes (4, 30).

14. In reference to claim 19, figure 6 of Aritome shows that there is a second gate insulating film (33) on the inner surface of each of the second trenches.

15. Claims 4, 7-11, 14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara (JP 2001-274367).

16. In reference to claim 4, Hagiwara (JP 2001-274367) discloses a similar device. Figure 29 discloses a non-volatile semiconductor memory device with memory cells arranged in a matrix on a semiconductor substrate (100). Each cell in the matrix has a floating gate or electrode (140). A plurality of first trenches are formed in the semiconductor substrate (100) with each first trench being formed between the memory cells adjacent each other along a gate width direction. The plurality of first trenches is filled with an isolating filler (110). There is a plurality of second trenches formed in the isolating filler between the floating gates (140) of the memory cells adjacent to each other along the gate width direction. A word line (160), buried in the second trenches, is connected to the memory cells and extends along the gate width direction. Hagiwara does not each the exact trench shape as claimed by the applicant. However:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Therefore this claim is not patentable over Hagiwara.

17. In reference to claim 7, figure 29 of Hagiwara shows a gate insulating film (150) in the second trenches. The wordline (160) is on the gate insulating film (150).

18. With regard to claim 8, Hagiwara discloses that the gate insulating film (150) may be made of silicon nitride (paragraph 45).

19. In reference to claim 9, the first and second trenches of Hagiwara have approximately the same top diameter. However the second trench of Hagiwara has bottom diameter which is smaller than that of the first trench. Thus Hagiwara has ratio of a top diameter to a bottom diameter of the second trench which is greater than the ratio of a top diameter to a bottom diameter of the first trench.

20. In reference to claim 10, the second trench is shallower than the first trench and extends below a surface of the semiconductor substrate (100).

21. With regard to claim 11, the non-volatile memory device in figure 29 is a NOR type electrically erasable programmable read only memory (paragraph 9).

22. In reference to claim 18, figure 6 of Hagiwara shows that there is a second gate insulating film (150) on the inner surface of each of the second trenches.

23. With regard to claim 21, the applicant has characterized a second trench which is capable of reducing parasitic capacitance as being shallower than the first trench and preferably reaches at least the surface of the well region (currently filed specification, p. 9, lines 16-21). The second trench of Hagiwara meets these characteristics thus

meeting the claim. Furthermore, the applicant has characterized a second trench as reducing parasitic capacitance since the parasitic capacitance generated by the floating gate, the dielectric in the trench, and an insulating film of the trench, and at the word line is electrically connected in parallel to the parasitic capacitance between floating gates of the memory cells (currently filed specification, p. 3, lines 6-16). The second trench of Hagiwara also meets these characteristics as well and thereby meets the claim.

24. In reference to claim 14, Hagiwara (USPN 5,949,101) discloses a similar process. Figure 29 of Hagiwara discloses a method of manufacturing a semiconductor memory which comprises making element isolating regions (110) by forming a plurality of first trenches in a semiconductor substrate (100). Each first trench is made between adjacent ones of memory cell forming regions along a gate width direction. The plurality of first trenches is filled with a plurality of isolating fillers. A plurality of floating gate electrodes (140) are formed on the semiconductor substrate (100) at the memory cell forming regions. The floating gate electrodes (140) have a predetermined gate width. A plurality of second trenches is formed in the isolating fillers filled in the first trenches. Each second trench is made between adjacent ones of the floating electrodes (140) along the gate width direction. A word line (160) is formed in the second trenches. The wordline (160) is connected to the memory cells and extends along the gate width direction. Hagiwara does not each the exact trench shape as claimed by the applicant. However:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Therefore this claim is not patentable over Hagiwara.

25. With regard to claim 16, the second trenches are in self-alignment with the floating electrodes (140).

26. In reference to claim 19, figure 29 of Hagiwara shows that there is a second gate insulating film (33) on the inner surface of each of the second trenches.

Allowable Subject Matter

27. Claims 5, 15, and 22 were allowed in a previous Office action.

28. The following is an examiner's statement of reasons for allowance: the reasons for the allowance of claims 5, 15, and 22 were cited in a previous Office action.

29. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin Quinto/
Examiner, Art Unit 2826

/Sue A. Purvis/

Supervisory Patent Examiner, Art Unit 2826